IN THE CLAIMS:

Please amend the claims as follows:

Claims 1 - 15 (Cancelled)

16. (New) A common memory controller capable of controlling different types of memory chips, comprising:

a first interface portion for receiving a control output signal to access said memory chip from a controller, and outputting a control input signal to the controller;

a conversion control portion for converting said control output signal into a memory input signal in response to a specification of a memory chip to which the memory controller is connected, and converting a memory output signal output from the memory chip into the control input signal receivable to said controller;

a second interface portion for outputting the memory input signal and receiving the memory output signal; and

a plurality of terminals coupled to the second interface portion, and capable of connecting at least one of the different types of memory chips.

17. (New) The common memory controller according to claim 16, wherein the different types of memory chips include a synchronous DRAM or a synchronous SRAM.

18. (New) The common memory controller according to claim 16, further comprising

a memory unit for storing the specification of the memory chip, and wherein the memory unit is programmable.

19. (New) The common memory controller according to claim 16, wherein the specification of memory chip includes a memory type, a command sequence, an address sequence or latency information.

20. (New) The common memory controller according to claim 16, wherein the second interface unit controls an output timing of the memory input signal in response to the specification of memory chip.

21. (New) The common memory controller according to claim 16, wherein the memory input signal includes an address, a command, and data.

22. (New) The common memory controller according to claim 21, wherein the memory input signal further includes a chip select signal.

23. (New) The common memory controller according to claim 21, wherein the memory input signal further includes a direct memory access control signal.

24. (New) The common memory controller according to claim 16, wherein the number of the plurality of terminals is larger than that of the terminals of each of the memory chips to which the memory controller is connected.

25. (New) The common memory controller according to claim 16, wherein the plurality of terminals include control terminals, address terminals, data terminals, and a clock terminal.

26. (New) A multi chip package comprising:

a system LSI chip including a common memory controller capable of controlling different types of memory chips; and

a memory chip coupled to the system LSI chip, and controlled by the common memory controller,

the common memory chip including:

a first interface portion for receiving a control output signal to access said memory chip from a controller of the LSI chip, and outputting a control input signal to the controller;

a conversion control portion for converting said control output signal into a memory input signal in response to a specification of the memory chip, and converting a memory output signal from the memory chip into the control input signal receivable to said controller;

a second interface portion for outputting the memory input signal and receiving the memory output signal; and

a plurality of terminals coupled to the second interface portion, for connecting the memory chip.